A Class-AB Output Buffer for Driving High Capacitive Loads

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Abstract

A rail-to-rail 1.8V CMOS Op-Amp is presented in this paper. The Op-Amp has a class-AB output stage to drive large capacitive loads up to 2nF off-chip. The buffer is capable of driving resistive loads as low as 200Ω with acceptable THD. The Op-Amp, implemented in 0.18μm CMOS single-poly six-metal layers, has an open-loop gain of 50 dB, 60° phase margin and 4.1 MHz unity gain bandwidth.

Keywords:*High drive buffer; opamp; output buffer*

1. Introduction

CMOS OpAmps are used extensively in wide variety of applications such as switched capacitor filters which needs to drive low capacitive loads. In the mixed-signal and some analog designs such as multilayer neural networks, a high drive buffer is needed. In these applications the number of external connections differs from application to application, which changes the loading condition of the chip over a wide range. Therefore, the design of such a high drive buffer has different constrains from those of low power or general purpose OpAmps. A high drive buffer is needed to drive capacitive loads up to 1nF or higher and low resistive loads down to 1KΩ or lower with proper phase margin, slew rate and total harmonic distortion. Low quiescent current, small die area and high linearity are some of the important design issues.

There are many reported works to solve the OpAmp problems , but unfortunately most of them have limitations such as low capacitive load handling [1,7], high standby power consumption [6, 5], or area consuming and complex designs[4, 2].

This paper presents a feed-forward, class-AB control biasing output buffer, for driving heavy loads. Section 2 describes the operation of the proposed output stage. Section 3 presents the Op-Amp realization and experimental results. Conclusions are given in Section 4.

2. Circuit Description

Figure 1 shows the class-AB OpAmp. Device geometries are given in Table 1. In order to maintain a rail to rail input stage, two pairs of complementary differential pairs, M1-M2 and M3-M4 are used. In order to reduce the g_m variations over the common mode input range, the level shifting technique is used [7, 8]. The transistors, M7 to M10, are used to overlap the transition region of the differential pairs to provide a rather constant transconductance. M5 and M6 are used to provide the input current for the input transistor pairs. M11 to M14 are used for biasing.

The currents of the differential inputs are added together through M15 to M18. To provide a large enough gain at the output while keeping the input-output swing high, a folded cascode stage, M19 to M26, is used.

The intermediate stage consists of two common-drain configurations, M27-M28 and M29-M30, to provide the biasing for the output transistors. This does not contribute to the gain, but rather provides a constant voltage difference between the output transistors' gates for class-AB biasing. To increase the maximum drive of the output transistors, variable loads are used at their gates. In quiescent condition, M33 and M34 are in saturation region, which reduces the load seen at the gate of the output transistor. When V_{in} increases, M34 goes from saturation to linear , causing the overall resistance at the gate of the output transistor to increase and allowing the voltage swing to become large enough for maximum drive. Similarly when the input decreases, M31 goes to linear region, and drives the N-transistor at the output with maximum drive.

Miller compensation [3] using two capacitors can be used to provide stability while driving high capacitive loads. However, for driving heavy capacitance load of 1nF or higher, the compensation capacitor values should be large, which increases the die area of the buffer. Miller zero compensation scheme is used to avoid having two capacitors for compensation. M35-M36 are used as resistors for compensation. A careful choice for (W/L) ratio of these transistors changes the

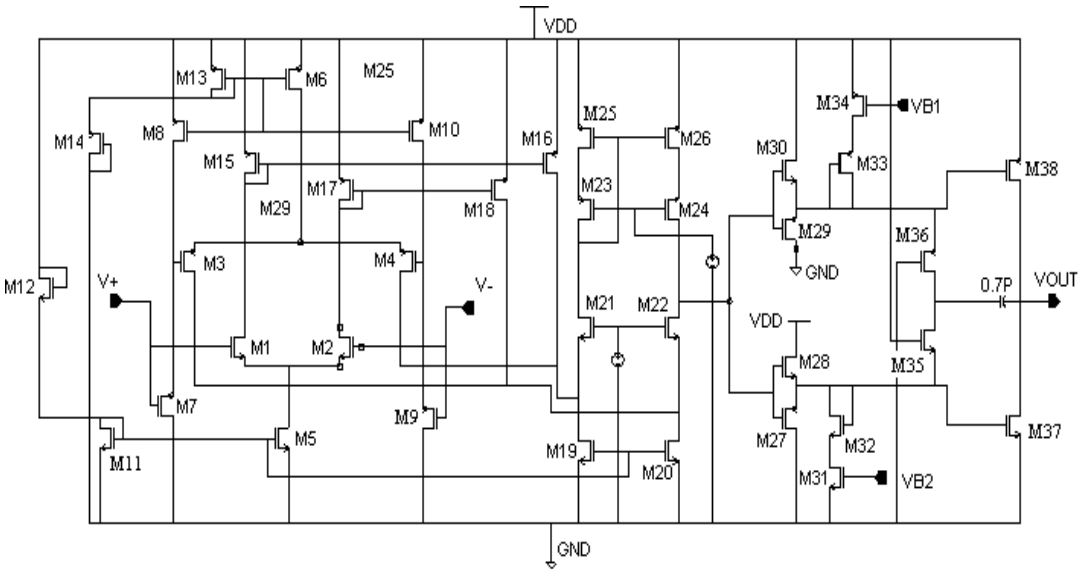

Figure 1: Full schematic of Op-Amp circuit

related poles and zeros of the system to maintain an acceptable gain and phase margin. These transistors also reduce the impedance seen at the gates of the output transistors, and shift the poles generated by C_{gd} of the output transistors to the higher frequencies. A compensation capacitor of 0.7pF is used which is a relatively small capacitor. The proposed output stage has a compact structure with good control on the quiescent current and drive capability.

3. Experimental Results

The buffer was realized in a 0.18μ single-poly six metal p-well CMOS process. The design occupied $4136\mu m^2$. Simulations showed that the g_m variation was within $\pm 5\%$ by using this technique. Figure 2 illustrates the output voltage when common mode input is changing from 0 to 1.8V.

Figure 3 shows the push and pull currents of the output transistors. The (W/L) ratio of the output NMOS is 18/0.7 and that of the PMOS is 81/0.7. The quiescent current is only $18\mu A$, while the push or pull current of the output transistors is about $760\mu A$.

The buffer has good phase margin for capacitive loads from 27pF up to 2nF. Figure 4 shows the magnitude and phase responses of the buffer while driving a 2nF capacitive load. It has 60° phase margin, open-loop gain of 50dB and 4.1MHz unity gain bandwidth.

The circuit is able to drive loads as low as 2KΩ from rail to rail. Figure 5 illustrates the measured output voltage when the differential input is swept between

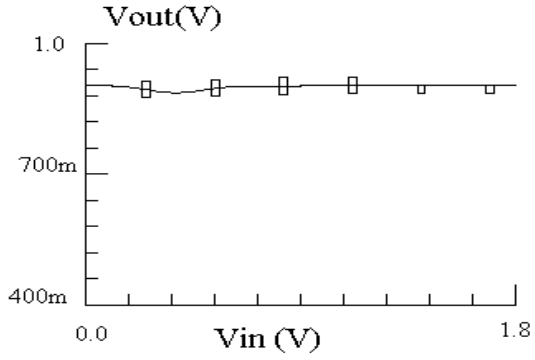

Figure 2: Op-Amp output voltage variations

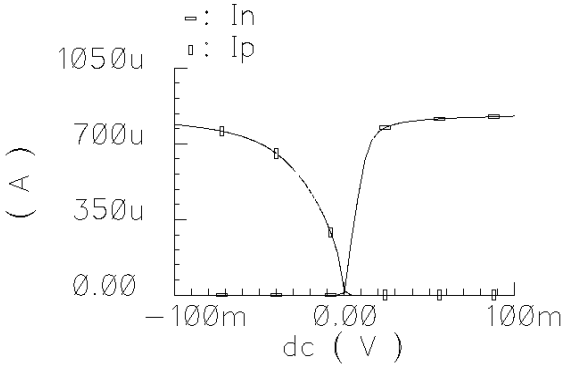

Figure 3: Push and pull currents of the output transistors

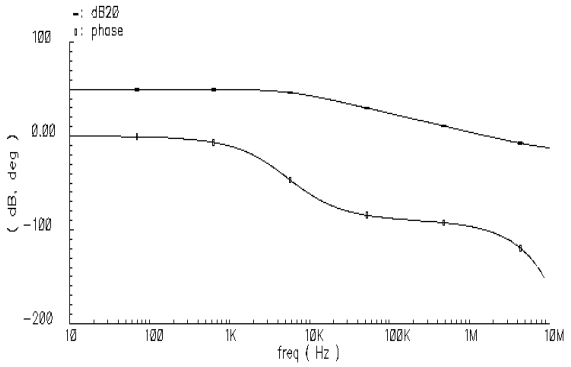

Figure 4: Magnitude and phase response for a 2nF load

-100mV and 100mV for two different resistive loads of 10KΩ and 200Ω. DC offset voltage is $150\mu V$. Total harmonic distortion when 1KHz sine wave with 1V p-p was applied to the buffer while driving a 200Ω load was 0.2%.

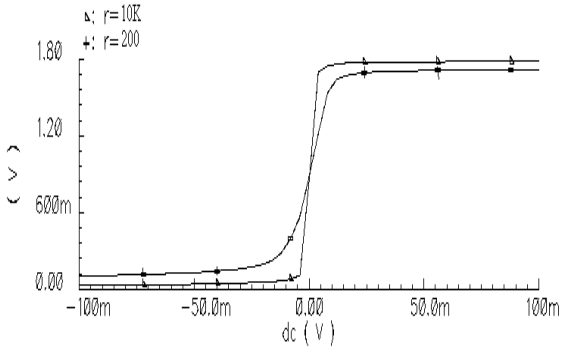

Figure 5: Measured output DC voltage

The Op-Amp was used in a unity-gain follower configuration. Figure 6 shows the transfer characteristics of the buffer for two different loads of $10K\Omega$ and 200Ω. With loads as low as 200Ω output swing is still around 80% of the power supply.

A 1V pulse step input has been applied to the Op-Amp in the unity gain follower configuration. No oscillations were observed as shown in Figure 7 for a 10KΩ and 2nF load, which ensures the stability of the buffer. The slew rate of the Op-Amp while driving 2nF capacitive and 10KΩ resistive load was 0.7 V/μs. The slew rate is up to 5V/μs for capacitive loads as low as 40pF and 10KΩ resistive load.

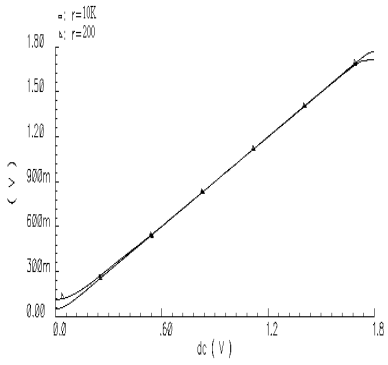

Figure 6: Transfer characteristics of the opamp with different resistive loads

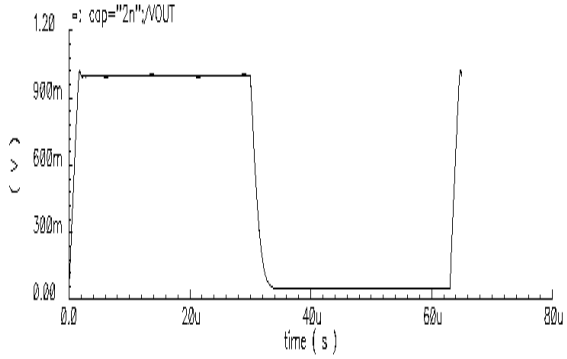

Figure 7: Pulse response for 2nF load

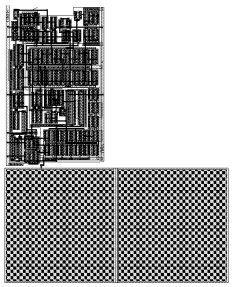

Figure 8: Buffer layout

4. Conclusion

A 1.8V CMOS Op-Amp with constant g_m and rail-to-rail input and output stages was reported. Op-Amp was realized in $0.18\mu m$ single-poly six-metal layers p-well CMOS process. The simulation results showed the stability of the Op-Amp for a wide range of capacitive loads. A high ratio between the maximum and quiescent currents was observed. The low quiescent current of only 18μA makes this circuit a suitable choice for low-power mixed-signal designs.

Transistor	*(W/L) ratio*
M_1, M_2	12/0.7
M_3, M_4	48/0.7
M_5, M_{11}	4/0.7
M_6, M_{13}	10/0.7
M_7, M_9	7/0.32
M_8, M_{10}	1/0.32
M_{12}	0.5/1.1
M_{14}	1.8/2.3
$M_{15}, M_{16}, M_{17}, M_{18}$	5/0.7
M_{19}, M_{20}	6/0.7
M_{21}, m_{22}	4/0.7
M_{23}, M_{24}	7/0.7
M_{25}, M_{26}	7/0.7
M_{27}	10/0.7
M_{28}	20/0.7
M_{29}	15/0.7
M_{30}	8/0.7
M_{31}, M_{32}	3/0.7
M_{33}, M_{34}	10/0.7
M_{35}	0.4/14
M_{36}	0.4/10
M_{37}	18/0.7
M_{38}	90/0.7

Table 1- Transistors aspect ratios

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Class A and class AB operational amplifiers are an essential part of a mixed- signal chip, where they are used as active filter sub-blocks, compensators, reference current generators and voltage buffers, to name just a few of many applications. For analog circuits such as operational amplifiers a mixed-signal chip is a very unfriendly operating environment, where the power supply is often corrupted by high current switching circuits.Â IV Loikkanen M & and Kostamovaara J (2005) Improving capacitive drive capability of two-stage op amps with current buffer. Proceedings of the European Conference on Circuit Theory and Design 1: 99â€“102. V Loikkanen M & Kostamovaara J (2006) PSRR improvement technique for ampliers with miller capacitor. Therefore, the output buffer amplifier has a good driving capability when the capacitive load is larger and the voltage swing of the input transient response is higher. The proposed buffer amplifier can provide a substantial slew rate enhancement during a full-swing transition for high voltage, as conventional buffer amplifiers do.Â A high-speed, low-power, rail-to-rail, folded-cascode, class-AB output buffer amplifier with an adaptive biasing circuit is proposed. The proposed buffer amplifier uses a compact, novel, adaptive biasing scheme for a slew rate enhancement. To obtain a faster transient response, the proposed adaptive biasing scheme requires just two transistors of the additional tail current sources and eight transistors for current mirrors. When a capacitive load must be driven, a further increase (overcompensation) can increase stabilityâ€“but at the expense of bandwidth. Q. So far you've only discussed voltage feedback op amps exclusively, right? Do current feedback (CF) op amps behave similarly with capacitive loading? Can I use any of the compensation techniques discussed here? A. Some characteristics of current feedback architectures require special attention when driving capacitive loads, but the overall effect on the circuit is the same. The added pole, in conjunction with op-amp output resistance, increases phase shift The Op-Amp has a class-AB output stage to drive large capacitive loads up to 2nF off-chip. The buffer is capable of driving resistive loads as low as 200â„¦ with acceptable THD. The Op-Amp, implemented in 0.18µm CMOS single-poly six-metal layers, has an open-loop gain of 50 dB, 60â— phase margin and 4.1 MHz unity gain bandwidth. Figure 1 shows the class-AB OpAmp.Â Miller compensation [3] using two capacitors can be used to provide stability while driving high capacitive loads. However, for driving heavy capacitance load of 1nF or higher, the compensation capacitor values should be large, which increases the die area of the buffer. Miller zero compensation scheme is used to avoid having two capacitors for compensation.